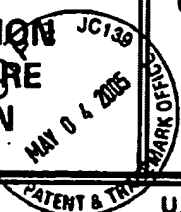


INFORMATION DISCLOSURE CITATION PTO-1449		CUSTOMER NUMBER 45114		ATTORNEY'S DKT No. H1420		APPLICATION No. 10/754,559	
				APPLICANT(S) Shibly S. Ahmed et al.			
				FILING DATE January 12, 2004		GROUP 2812	


U.S. PATENT DOCUMENTS


EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
R	6,764,884 B1	07/20/04	Yu et al.	438	157	—
	6,465,823	10/15/02	Yagishita et al.	257	288	—
	6,765,303 B1	07/20/04	Krivokapic et al.	257	903	—
	6,509,611 B1	1/21/03	Park et al.	257	330	—
	2002/0177263 A1	11/28/02	Hanafi et al.	438	183	—
✓	2002/0153587 A1	10/24/02	Adkisson et al.	257	510	—

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No
R	EP 1 383 164 A1	01/21/04	Europe	—	—	✓	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

R	Copy of International Search Report dated March 4, 2005

EXAMINER 	DATE CONSIDERED 7/16/05
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INFORMATION DISCLOSURE CITATION PTO-1449		Customer Number: 26615	ATTORNEY'S DKT No. H1420	APPLICATION No. Unassigned 60/75459	
			APPLICANT(S) Shibly S. Ahmed et al.		
			FILING DATE January 12, 2004	GROUP Unassigned 2818	

U.S. PATENT DOCUMENTS						
EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
R	6,583,469	06-24-03	Fried et al.	257	329	01-28-02
J	6,562,685	05-13-03	Yu	438	149	10-16-00
J	6,551,886	04-22-03	Yu	438	300	04-27-01

FOREIGN PATENT DOCUMENTS							
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No
R	WO 03/015182	02-03	WIPO	—	—	✓	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)	
R	Digh Hisamoto et al., "FinFET-A Self-Aligned Double-Gate MOSFET Scalable to 20 nm," IEEE Transactions on Electron Devices, Vol. 47, No. 12, December 2000, pages 2320-2325.
R	Yang-Kyu Choi et al., "Sub-20nm CMOS FinFET Technologies," 2001 IEEE, IEDM, pages 421-424.
J	Xuejue Huang et al., "Sub-50 nm P-Channel FinFET," IEEE Transactions on Electron Devices, Vol. 48, No. 5, May 2001, pages 880-886.
J	Xuejue Huang et al., "Sub 50-nm FinFET: PMOS," 1999 IEEE, IEDM, pages 67-70.
J	Yang-Kyu Choi et al., "Nanoscale CMOS Spacer FinFET for the Terabit Era," IEEE Electron Device Letters, Vol. 23, No. 1, January 2002, pages 25-27.
J	Co-pending U.S. Application No. 10/320,536 filed December 17, 2002 entitled: "FinFET Gate Formation Using Reverse Trim of Dummy Gate," 14 page specification, 11 sheets of drawings.
J	Co-pending U.S. Application No. 10/459,589 filed June 12, 2003 entitled: "FinFET Gate Formation Using Reverse Trim and Oxide Polish," 17 page specification, 28 sheets of drawings.
J	Co-pending U.S. Application No. 10/310,777 filed December 6, 2002 entitled: "Damascene Gate Process with Sacrificial Oxide in Semiconductor Devices," 19 page specification, 10 sheets of drawings.
J	Co-pending U.S. Application No. 10/645,577 filed August 22, 2003 entitled: "Sacrificial Oxide Protection During Dummy Gate Removal in Damascene Gate Process in Semiconductor Devices," 19 page specification, 9 sheets of drawings.

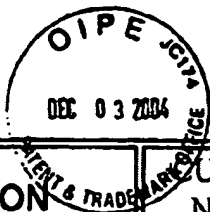
EXAMINER 	DATE CONSIDERED 7/16/05
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SHEET 1 OF 1

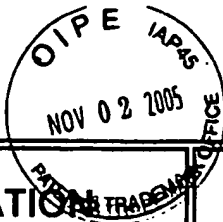
INFORMATION DISCLOSURE CITATION PTO-1449	CUSTOMER NUMBER 26615	ATTORNEY'S DKT No. H1420		APPLICATION No. 10/754,559			
		APPLICANT(S) Shibly S. Ahmed et al.					
		FILING DATE January 12, 2004		GROUP 2812			
U.S. PATENT DOCUMENTS							
EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE	
RL	6,396,108	05/28/02	Krivokapic et al.	257	365	—	
RL	5,801,397	09/01/98	Cunningham	257	66	—	
FOREIGN PATENT DOCUMENTS							
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)							
RL	Stephen H. Tang et al., "Comparison of Short-Channel Effect and Offstate Leakage in Symmetric vs. Asymmetric Double Gate MOSFETs", IEEE International SOI Conference, October 2000, pp. 120-121						
RL	Co-pending U.S. Application No. 10/720,166 filed November 25, 2003 entitled: "Damascene Gate Process with Sacrificial Oxide in Semiconductor"; 19 page specification, 10 sheets of drawings.						
RL	Co-pending U.S. Application No. 10/838,228 filed May 5, 2004 entitled: "Sacrificial Oxide for Minimizing Box Undercut in Damascene FinFet"; 15 page specification, 12 sheets of drawings.						
RL	United States Patent Application Publication No. US2002/0153587; publication date October 24, 2002; Adkisson et al.						
EXAMINER <i>Charles</i>				DATE CONSIDERED <i>7/16/05</i>			

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INFORMATION DISCLOSURE CITATION PTO-1449		CUSTOMER NUMBER 26615		ATTORNEY'S DKT NO. H1420		APPLICATION NO. 10/754,559	
				APPLICANT(S) Shibly S. Ahmed et al.			
				FILING DATE January 12, 2004		GROUP 2812	
U.S. PATENT DOCUMENTS							
EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE	
✓	6,645,797 B1	11/2003	Buynoski et al.	438	157	—	
FOREIGN PATENT DOCUMENTS							
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)							
EXAMINER <i>Uha</i>				DATE CONSIDERED <i>7/16/05</i>			

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		APPLICANT(S) Shibly S. Ahmed et al.					
		FILING DATE January 12, 2004	GROUP 2818				
U.S. PATENT DOCUMENTS							
EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE	
<i>TV</i>	6,855,990	02/2005	Yeo et al.	257	353	—	
FOREIGN PATENT DOCUMENTS							
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)							
EXAMINER <i>Thao</i>				DATE CONSIDERED <i>11/04/05</i>			

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